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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,265	07/22/2004	Michitaka Kameyama	81919.0020	9388

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,265	KAMEYAMA ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *1-3,8-11 and 14* is/are rejected.

7)☒ Claim(s) *4,6,7,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of copending Application No. 10/889,402. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims essentially comprise the same recitations.

Claims 1-3 of the instant application recite fewer limitations than what recited in claims 1-3 of application 10/889,402.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

3. Claims 6 and 7 are objected to because of the following informalities: it is not clear of the dependency of claims 6 and 7. In claims 11 and 12, replace anyone of claims to claim. Also in claim 11, change "...are arranges..." to either "...is arranged..." or "...are arranged...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 8-11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimori (US 2005/00177757)

The applied reference has a common assignee or inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 1, Fujimori teaches all claimed features in Figs. 1-6, a logical operation circuit comprising: a ferroelectric capacitor (CF1) which can retain a polarization state

(P1) corresponding to first operation target data (y1) and which has first (3) and second (5) terminals; a first signal line (7) connected to the first terminal (3); a second signal line (9) which can provide second operation target data (y2) to the second terminal of the ferroelectric capacitor retaining the polarization state corresponding to the first operation target data (when y1 and y2 having the same logical value) and which is connected to the second terminal (5); and an operation result output section (MP) which outputs the result of a logical operation (Fig. 7A or 7B) on the first and second operation target data based on a polarization state of the ferroelectric capacitor generated by providing the second operation target data to the ferroelectric capacitor and which is connected to the first signal line.

In claim 2, Fujimori further teaches the logical operation circuit as set forth in Claim 1, wherein the first and second signal lines are connected to one of first and second reference potentials (3 or 7 connected to ground and 5 or 9 connected to Vdd, as shown in Fig. 3A) and the other of the first and second reference potentials, respectively, to generate the polarization state corresponding to the first operation target data in the ferroelectric capacitor (P1 or P2 is shifting to P3).

In claim 3, Fujimori further teaches the logical operation circuit as set forth in Claim 1 or 2, wherein the operation result output section has an electric field effect transistor (MP) as an output transistor which has a gate terminal connected to the first signal line (7) and an output terminal (ML) for outputting an output signal corresponding to a control signal inputted into the gate terminal, and which becomes off when a

potential on the first reference potential side from its threshold voltage is given (when the control signal at the gate of MP is at logic 0) as the control signal and becomes on when a potential on the second reference potential side from its threshold voltage is given as the control signal (when the control signal at the gate of MP is at logic 1), and wherein the result of the logical operation is obtained as an output signal (on ML) from the output transistor.

In claim 8, Fujimori teaches all claimed features in Figs. 1-7, a logical operation circuit comprising: a non-volatile memory element (CF1) which can retain a non-volatile state (store) corresponding to first operation target binary data y (y1) and which has first (3) and second (5) terminals; and an operation result output section (MP) which outputs, based on a state of the non- volatile memory element generated by providing second operation target binary data x (y2) to the second terminal (5) of the non-volatile memory element (CF1), the result of a logical operation (on ML) on the first and second operation target binary data x and y as result binary data z (ML), wherein the operation result binary data z substantially satisfies (Fig. 7A, when y1 = 1, y2 =2 then ML =1 satisfies) the following relation: z = x AND y.

In claim 9, Fujimori further teaches the logical operation circuit as set forth in Claim 8, wherein the non-volatile memory element includes a ferroelectric capacitor (CF1) and the non-volatile state is a residual polarization state (the residual polarization state P1 [0078]) of the ferroelectric capacitor.

Claim 10 corresponds to detailed circuitry already discussed similarly with regard to claim 8.

In claim 11, Fujimori further teaches in Fig. 9, the logical operation circuit as set forth in Claim 10 which is arranged in series and/or parallel to perform a desired operation (a EXOR b EXOR c).

Claim 14 corresponds to detailed circuitry already discussed similarly with regard to claim 8.

6. Claims 4, 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 5 appears to comprise allowable subject matter of the first and second signal lines are then both connected to the second reference potential to precharge the first signal line to the second reference potential without causing a change in the residual polarization state of the ferroelectric capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIBOL TAN
PRIMARY EXAMINER